

## 2-line IPAD™, EMI filter and ESD protection

### Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming:  
1.42 mm x 0.92 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging

### Complies with the following standards

- IEC 61000-4-2 level 4 on input pins
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- IEC 61000-4-2 level 1 on input pins
  - 2 kV (air discharge)
  - 2 kV (contact discharge)

### Applications

Where EMI filtering in ESD sensitive equipment is required:

- Mobile phones and communication systems
- Computers, printers and MCU Boards

### Description

The EMIF02-MIC02 is a highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 Flip Chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up 15 kV.

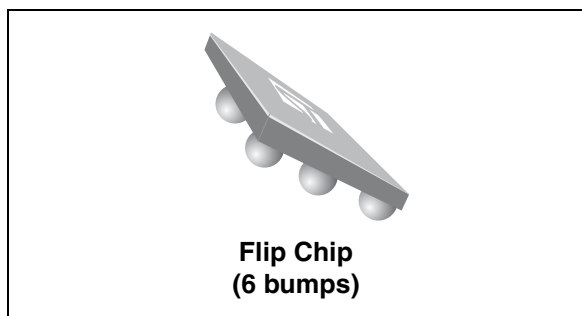


Figure 1. Pin configuration (bump side)

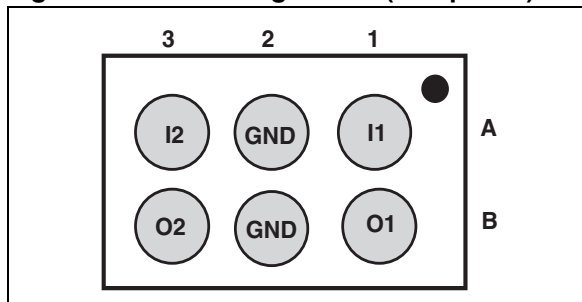
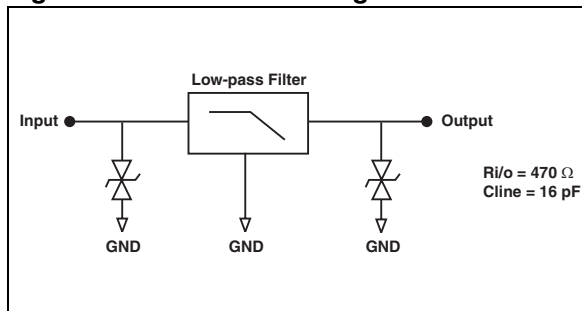


Figure 2. Basic cell configuration



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# 1 Electrical characteristics

**Table 1. Absolute ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameter	Value	Unit
$T_j$	junction temperature	125	$^{\circ}\text{C}$
$T_{op}$	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

Symbol	Parameters				
$V_{BR}$	Breakdown voltage				
$I_{RM}$	Leakage current @ $V_{RM}$				
$V_{RM}$	Stand-off voltage				
$V_{CL}$	Clamping voltage				
$R_d$	Dynamic impedance				
$I_{PP}$	Peak pulse current				
$R_{I/O}$	Series resistance between input and output				
$C_{line}$	Input capacitance per line				
Symbol	Test conditions				
$V_{BR}$	$I_R = 1\text{ mA}$	14	16		V
$I_{RM}$	$V_{RM} = 12\text{ V per line}$			500	nA
$R_{I/O}$		423	470	517	$\Omega$
$C_{line}$	@ 0 V		40	45	pF

Figure 3. S21 (dB) attenuation measurement and Aplac simulation

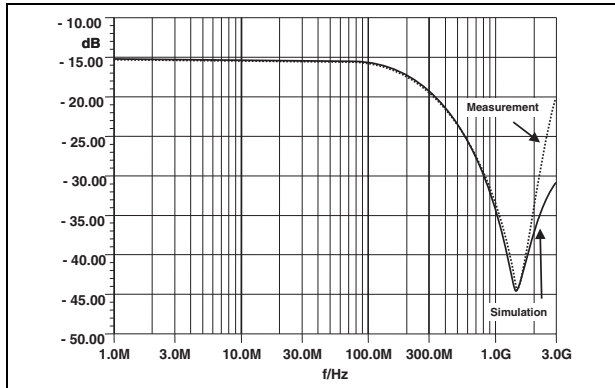


Figure 4. Analog crosstalk measurements

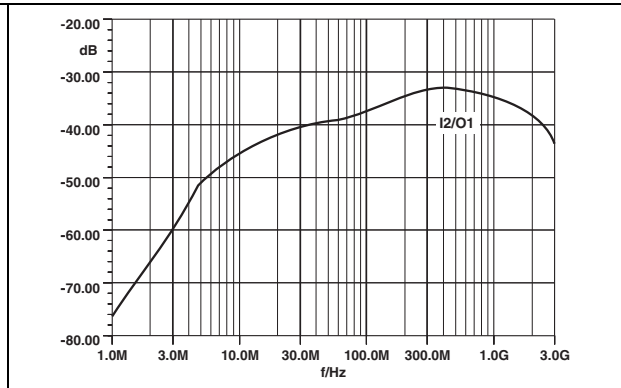


Figure 5. Digital crosstalk measurement

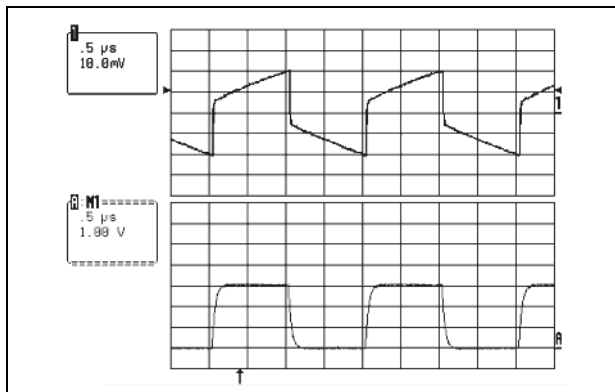


Figure 6. ESD response to IEC61000-4-2 (-15 kV air discharge) on one input V(in) and on one output (Vout)

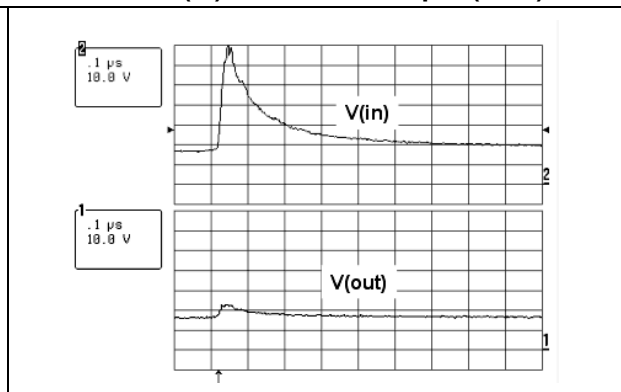


Figure 7. ESD response to IEC61000-4-2 (+15 kV air discharge) on one input V(in) and on one output (Vout)

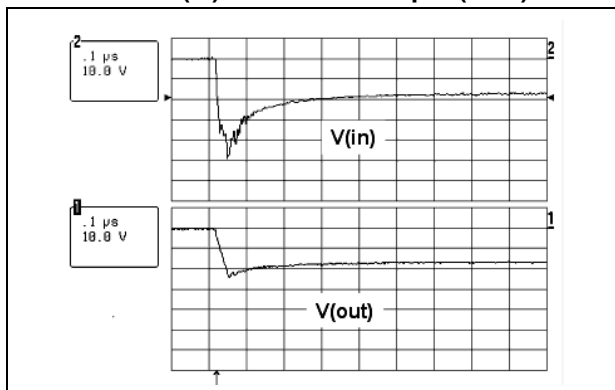
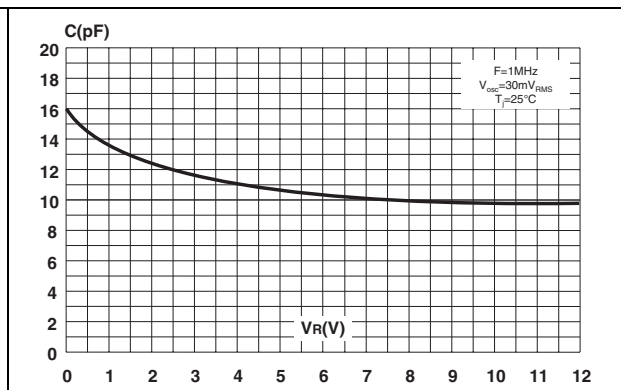
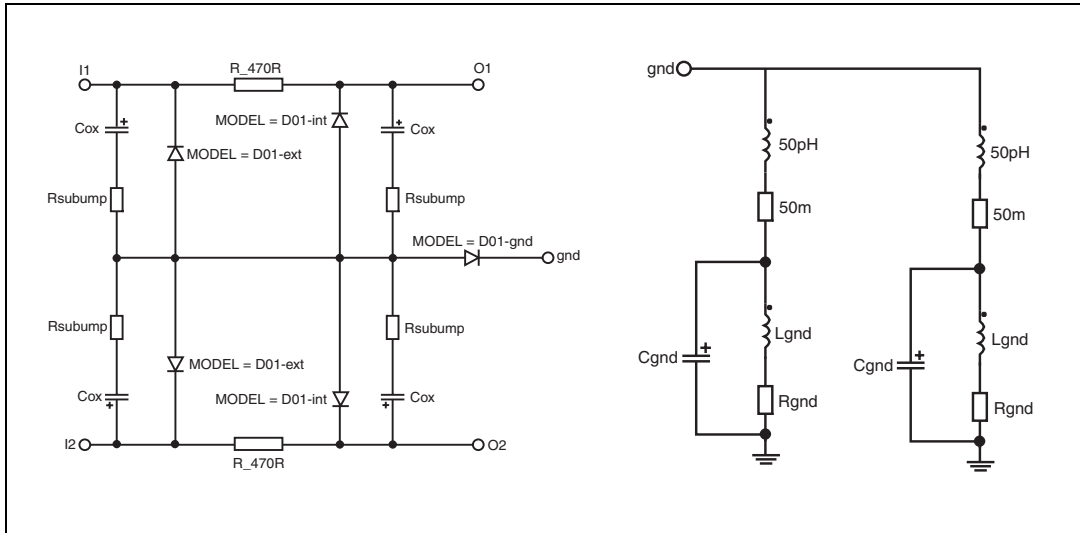


Figure 8. Line capacitance versus applied voltage



## 2 Application information

**Figure 9. Aplac model**

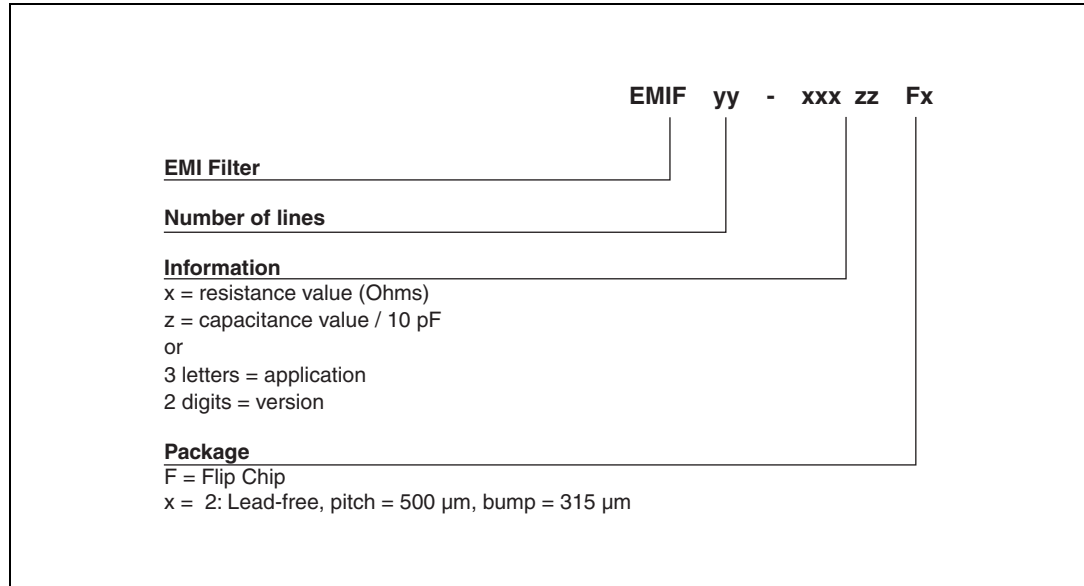


**Figure 10. Aplac parameters**

Model D01-ext	Model D01-int	Model D01-gnd	Ls 400pH
BV = 7	BV = 7	BV = 7	Rs 100m
CJO = Cz_ext	CJO = Cz_int	CJO = Cz_gnd	
IBV = 1u	IBV = 1u	IBV = 1u	R_470R 482.6
IKF = 1000	IKF = 1000	IKF = 1000	Cz_ext 8.73pF
IS = 10f	IS = 10f	IS = 10f	Rs_ext 850m
ISR = 100p	ISR = 100p	ISR = 100p	Cz_int 2.9pF
N = 1	N = 1	N = 1	Rs_int 850m
M = 0.3333	M = 0.3333	M = 0.3333	Cz_gnd 215.61pF
RS = Rs_ext	RS = Rs_int	RS = Rs_gnd	Rs_gnd 470m
VJ = 0.6	VJ = 0.6	VJ = 0.6	
TT = 50n	TT = 50n	TT = 50n	Rgnd 10m
			Lgnd 48pH
			Cgnd 0.15pF
			Cox 3.05pF
			Rsubump 200m

### 3 Ordering information scheme

Figure 11. Ordering information scheme



### 4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at [www.st.com](http://www.st.com).

Figure 12. Package dimensions

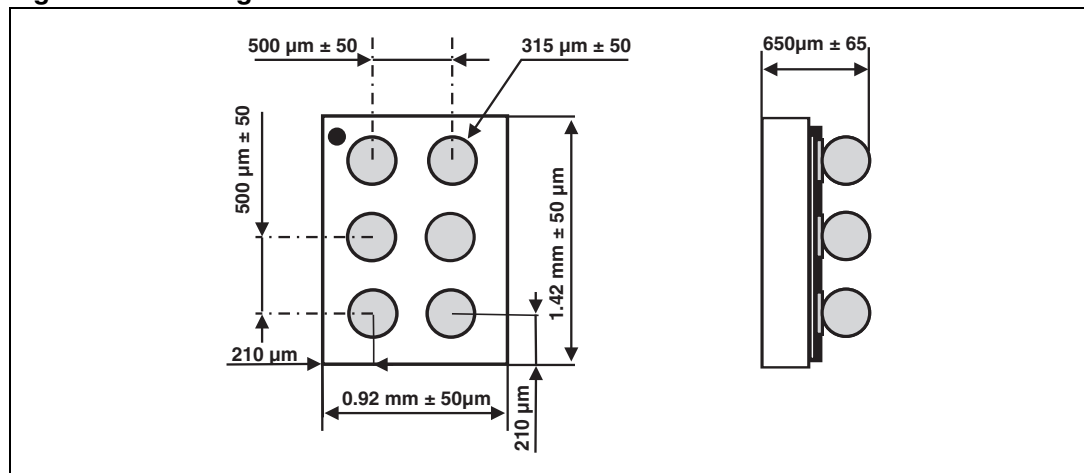


Figure 13. Footprint

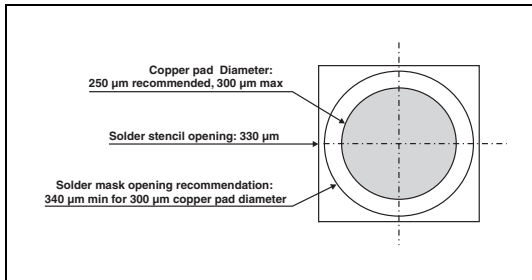


Figure 14. Marking

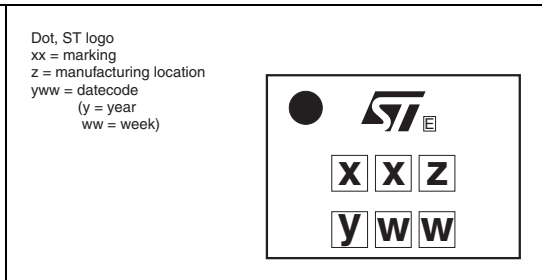
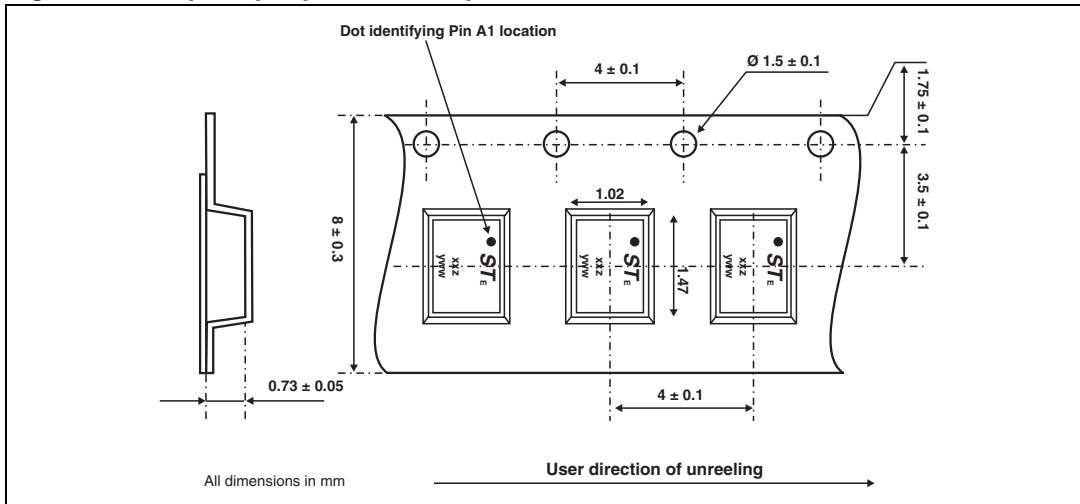


Figure 15. Flip Chip tape and reel specification



## 5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC02F2	FJ	Flip Chip	2.3 mg	5000	Tape and reel 7"

Note:

More information is available in the application notes:  
 AN1235: "Flip Chip: Package description and recommendations for use"  
 AN1751: "EMI filters: Recommendations and measurements"

## 6 Revision history

**Table 4. Document revision history**

Date	Revision	Changes
12-Oct-2004	1	Initial release.
11-Jan-2006	2	ECOPACK statement added. Die dimensions modified in <a href="#">Figure 12</a> . and first page. Typographical errors corrected.
17-Apr-2008	3	Updated ECOPACK statement. Updated <a href="#">Figure 11</a> , <a href="#">Figure 12</a> and <a href="#">Figure 15</a> . Reformatted to current standards.

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